**Digital Design and Computer Organization Laboratory**

**UE19CS206**

**3rd Semester, Academic Year 2020-21**

Date: 17/11/2020

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Experiment Number: 8 Week # : 8

**Title of the Program:** Microprocessor - 2

**Code:**

module control\_logic (input wire clk, reset, input wire [15:0] cur\_ins, output wire [2:0] rd\_addr\_a, rd\_addr\_b, wr\_addr, output wire [1:0] op, output wire sel, jump, pc\_inc, load\_ir, wr\_reg);

// Copy your assignment 3 logic here and modify.

wire u,w,s,wr\_reg1,wr\_reg2,alu\_ins,ld\_ins,ld\_ins\_,fi,fo,el,eo,ef ;

assign rd\_addr\_a=cur\_ins[2:0];

assign rd\_addr\_b=cur\_ins[5:3];

assign wr\_addr=cur\_ins[8:6];

assign op = cur\_ins[10:9];

invert i1(cur\_ins[15],u);

invert i2(cur\_ins[10],w);

invert i3(cur\_ins[14],s);

invert i4(ld\_ins,ld\_ins\_);

and2 a1(cur\_ins[15],s,ld\_ins);

nor5 n5({cur\_ins[15],cur\_ins[14],cur\_ins[13],cur\_ins[12],cur\_ins[11]},alu\_ins);

and3 a2(cur\_ins[14],u,ef,jump);

dfrl d1(clk,reset,1'b1,fo,eo);

and2 a3(ld\_ins\_,eo,ef);

and2 a4(ef,alu\_ins,wr\_reg1);

or2 o3(wr\_reg1,wr\_reg2,wr\_reg);

and2 a5(eo,ld\_ins,el);

and2 a6(ld\_ins,el,wr\_reg2);

nand2 n1(el,ld\_ins,sel);

dfrl d2(clk,reset,1'b1,el,lo);

or2 o1(lo,ef,fi);

dfsl d3(clk,reset,1'b1,fi,fo);

assign load\_ir = fo;

or2 o2(load\_ir,el,pc\_inc);

endmodule

**Output waveform**

